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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/672,637	09/28/2000	Gary Dan Dotson	00AB152	8211

7590 06/17/2005

Allen-Bradley Company, Inc.
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EXAMINER	
YANG, RYAN R	

ART UNIT	PAPER NUMBER
2672	

DATE MAILED: 06/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/672,637	DOTSON ET AL.	
	Examiner	Art Unit	
	Ryan R. Yang	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 9-20* is/are rejected.

7)☐ Claim(s) *5-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to communications: Amendment, filed on 3/1/2005. This action is final.

2. Claims 1-20 are pending in this application. Claim 1 is independent claim. In the Amendment, filed on 3/1/2005, claim 1 was amended.

3. The present title of the invention is "Raster engine with multiple color depth digital interface" as filed originally.

Claim Rejections - 35 USC § 103

4. Claims 1 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takebe (US 5,898,442) and further in view of Atsatt et al. (US 6,750,876).

5. As per claim 1, Takebe discloses raster engine for interfacing a frame buffer in a computer system to one of a plurality of disparate displays, comprising:

at least one control register programmable via the computer system to select a display mode (Figure 2, item 1 is the CRT Controller where the display 2 can be an EL, liquid crystal display, or other flat display, column 3, line 24-25);

a dual port RAM device operative to obtain pixel data from the frame buffer ("The frame memory 4 comprises dual port RAM", column 5, line 54); and

a logic device having a parallel output, the logic device being adapted to select appropriate pixel data from the dual port RAM device according to the selected display mode, and to remap the selected pixel data according to the selected display mode

(Figure 8 where the memory M1 is partitioned into n section and are parallel output and the Bus Selector 7 does the remapping; "the system permits switching of the display selection signal DSEL between H and L state in according with the type of display used, so that specified circuit sections can be switched between EL display driver and liquid crystal display driver modes", column 5, line 40-44);

the raster engine provides the remapped selected pixel data at the parallel output via the logic according to a universal routing scheme applicable to the plurality of disparate displays (Figure 8, the bus selector 7 provides the remapping, display 2 is a display where the display can be an EL, liquid crystal display, or other flat display, column 3, line 24-25 and Figure 10 is a universal routing scheme).

Takebe discloses a raster engine for interfacing a frame buffer in a computer system to one of a plurality of disparate displays with a controller. It is noted that Takebe does not explicitly disclose the controller is a register programmable via the computer system to select a display mode, however, this is known in the art as taught by Atsatt et al., hereinafter Atsatt. Atsatt discloses a programmable display controller in which the "the video-mode-select bit(s) allow the programmable display controller 400 to operate in a plurality of video modes" (column 7, line 18-21).

Thus, it would have been obvious to one of ordinary skill in the art to incorporate the teaching of Atsatt into Takebe because Takebe discloses an interface for a plurality of disparate displays with display mode controller and Atsatt discloses the controller could be programmable in order to provide a selectable display format and to reduce the amount of storage space required in image memory (column 3, line 20-23).

6. As per claim 19, Takebe and Atsatt et al. demonstrated all the elements as disclosed in the rejected claim 1, and Takebe further discloses the logic device comprises a multiplexer (Figure 8, where the Bus Selector 7 is a multiplexer).

7. Claims 2-4 and 9-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takebe (US 5,898,442) in view of Atsatt et al., and further in view of Reddy et al., U.S. Patent No.: 6,215,459.

8. In regards to claim 2, Takebe and Atsatt et al. demonstrated all the elements as disclosed in the rejected claims 1.

Takebe and Atsatt et al. disclose an interface to a plurality of disparate displays. It is noted that Takebe and Atsatt et al. do not explicitly disclose the selected display mode as claimed, however, this is known in the art as taught by Reddy et al., hereinafter Reddy. Reddy discloses a 2x clock for displaying pixel data in a format of 1, 2, 4 or 8 bits per pixel (Col. 5, lines 13-28), where said 2x clock specifically is two pixels per clock. Since the applicant recites the "one of" language, Reddy reads on the limitations of the instant claim. In addition, the rest of the display mode as recited in the instant claim are standard display modes corresponding to a plurality of display devices and are comparable to said display more as taught by Reddy.

Thus, it would have been obvious to one of ordinary skill in the art to incorporate the teaching of Reddy into Takebe and Atsatt et al. because Takebe and Atsatt et al. disclose an interface to a plurality if disparate displays and Reddy discloses a display mode as claimed could be used in a plural display system in order to display a well known standard display mode.

9. In regards to claims 3 and 9, Takebe, Atsatt et al. and Reddy demonstrated all the elements as disclosed in the rejected claims 2 and 1, supra, respectively and Reddy further discloses et al. explicitly teaches a look-up table (FIG. 2), wherein the logic device receives the selected pixel data form the dual port RAM device via the look-up table as applied to claim 1 above.

Thus, it would have been obvious to one of ordinary skill in the art to incorporate the teaching of Reddy into Takebe and Atsatt et al. because Takebe and Atsatt et al. disclose an interface to a plurality if disparate displays and Reddy discloses a display mode as claimed could be used in a plural display system in order to display a well known standard display mode.

10. In regards to claim 10, Takebe and Atsatt et al. and Reddy demonstrated all the elements as disclosed in the rejected claim 1, supra, and Reddy further discloses a plurality of pixel modes and a 256 color mode comprising a look-up table mode as applied to claims 1-3 above. Reddy et al. also teaches a 2x clock, which specifically is a 2 pixels per pixel clock shift mode as applied to claims 1-3 above.

Thus, it would have been obvious to one of ordinary skill in the art to incorporate the teaching of Reddy into Takebe and Atsatt et al. because Takebe and Atsatt et al. disclose an interface to a plurality if disparate displays and Reddy discloses a display mode as claimed could be used in a plural display system in order to display a well known standard display mode.

11. In regards to claim 11, the same basis and rationale for claim rejection as applied to claims 3 and 10 above. Reddy et al. explicitly teaches a look-up table.

12. In regards to claims 12 and 16-17, the same basis and rationale for claim rejection as applied to claim 10 above. Reddy explicitly teaches 2X clock, which specifically is 2 pixels per shift clock.

13. In regards to claims 13-15, the same basis and rationale for claim rejection as applied to claims 1-3 above. Reddy et al. explicitly teaches 1, 2, 4, or 8 bits per pixel.

14. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takebe (US 5,898,442) in view of Atsatt et al., and further in view of Boger (6,326,935).

In regards to claim 20, Takebe and Atsatt disclose the raster engine of claim 1. It is noted that Takebe and Atsatt do not explicitly disclose a user interface for selecting a display mode, however, this is known in the art as taught by Boger. Boger discloses a user interface for selecting a display mode (Col. 6, line 62 – Col. 7, line 23), which specifically is a direct display command interface.

Thus, it would have been obvious to one of ordinary skill in the art to incorporate the teaching of Boger into Takebe and Atsatt because Takebe and Atsatt disclose an interface to a plurality if disparate displays and Boger discloses the user interface executed by a software in order to allow the user a direct access to changing the display mode.

15. In regards to claims 4 and 18, Takebe, Atsatt et al. and Reddy demonstrated all the elements as disclosed in the rejected claims 3 and 13, supra, and Takebe further discloses the logic device comprises a multiplexer (Figure 8, where the Bus Selector 7 is a multiplexer).

Allowable Subject Matter

16. Claims 5-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

17. The following is a statement of reasons for the indication of allowable subject matter:

In regarding claim 5, the applicant recites a logic device adapted to provide the selected pixel data to the output device in a 24 bit parallel format when the selected display mode is one of single 16 bit 565 pixel per clock and single 16 bit 555 pixel per clock. While it is well known in the art to display in a 24 bit parallel format, the prior art of record do not teach displaying in said 24 bit parallel format when selecting a single 16 bit 565/555 pixel per clock mode, which would be required in order to display the proper display mode corresponding to the selected output device.

Response to Arguments

18. Applicant's arguments, see Amendment, filed 3/1/2005, with respect to the rejection(s)of claim(s) 1 under Reddy et al., Ramamurthy and Boger have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Takebe (5,898,442).

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Inquiries

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan R Yang whose telephone number is (571) 272-7666. The examiner can normally be reached on M-F 9:30AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on (571) 272-7664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan Yang
June 12, 2005